Results **1** - **10** of about **19,800**. (**0.19** sec)

instruction set compiled **simulation**: a technique for fast and flexible **instruction set simulation** psu.edu [PDF]
M Reshadi, P Mishra, N Dutt - ... of the 40th annual Design Automation ..., 2003 - portal.acm.org
... The last bar is our **simulation** approach that uses both techniques: compile-time decode and using **templates** to produce optimized code. We have demonstrated that **instruction set** compiled sim- ulation coupled with our **instruction** abstraction technique delivers the performance **...**
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R Leupers, J Elste, B Landwehr - Proceedings of the ASP-DAC, 1999 - Citeseer
... While the number of dierent RT **templates** that may occur in **instruction-set** modelsis innite, the numberof primitiveoperations is limited. Therefore, a key compo- nent in Jacob is a xed library of **simulation** functions written inC,each ofwhichsimulatesoneprimitiveoper- ation. **...**
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An efficient retargetable framework for **instruction-set simulation** psu.edu [PDF]
M Reshadi, N Bansal, P Mishra, N Dutt - ... of the 1st IEEE/ACM/IFIP ..., 2003 - portal.acm.org
... IS-CS **simulation** technique in our retargetable framework by automatically extracting the required **templates** for simulating **...** EXPRESSION: A Language for Architecture Exploration through Compiler/**Simulator** Retargetability **...** [2] M.Reshadi et al, **Instruction-Set** Compiled **Simulation ...**
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[PDF] Automatic generation of microarchitecture **simulators** mtu.edu [PDF]
S Onder, R Gupta - IEEE International Conference on Computer ..., 1998 - cs.mtu.edu
... Specifies: - Micro-architecture. - **Instruction Set** Architecture (ISA). - Assembly language syntax and binary representation. **...** case s_MEM: dest=dcache[lmar]; end Specifying **Instruction** Syntax and Semantics Page 19. 19 **...** Disassembler **Template Simulator Template** ADL Compiler **...**
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A novel methodology for the design of application-specific **instruction-set** processors (ASIPs) using a machine description language psu.edu [PDF]
A Hoffmann, T Kogel, A Nohl, G Braun, ... - ... on computer-aided ..., 2001 - ieeexplore.ieee.org
... customizes a reduced **instruction-set** computer (RISC) processor within the Xtensa system [28]. **...** 2) extension of the target class of processors including single **instruction** multiple data **...** description of op- eration behavior including side effects for the **simulation** and implementation **...**
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A methodology for the design of application specific **instruction set** processors (ASIP) using the machine description language LISA whoiles.net [PDF]
A Hoffmann, O Schliebusch, A Nohl, G Braun, O ... - 2001 - computer.org
... As the system is based on an architecture **template** comprising quite a number of base instructions, it is far too **...** the LPDP system integrator platform provides a well defined ap- plication programming interface (API) to interconnect the **instruction-set simulator** generated from the **...**
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[PDF] SystemC cosimulation and emulation of multiprocessor SoC designs psu.edu [PDF]
L Benini, D Bertozzi, D Bruni, N Drago, F Fummi, M ... - IEEE Computer, 2003 - Citeseer
... (a) Figure 1. Archi- tectural **template** and **simulation** alternatives. (a) System functionali- ties are partitioned over a **set** of cores and other custom hardware (HW) blocks. (b) Full SystemC **simulation** implements all blocks as modules. (c) **Instruction-set simulator** (ISS)/ SystemC **...**
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An integer linear programming approach for identifying **instruction-set** extensions uci.edu [PDF]
C Ozturan, G Dundar, K Atasu - Third IEEE/ACM/IFIP ..., 2005 - ieeexplore.ieee.org
... A selection algorithm that ranks the generated **templates** based on isomorphism testing and potential eval- uation is described. **...** Machine description is updated automatically to support the **instruction-set** extensions. Extensive **simulation** results are presented. **...**
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NoCGEN: A **template** based reuse methodology for networks on chip architecture psu.edu [PDF]
J Chan, S Parameswaran - 2004 - computer.org
... Each router is connected via either directional or bidirectional point-to-point links. From a **template** topology such as a mesh, it is possible to add and remove links by editing the graph. **...** These can be as complex as an **instruction set simulator**. **...**
Cited by 43 - Related articles - All 8 versions

ASIP design methodologies: survey and issues psu.edu [PDF]
MK Jain, M Balakrishnan, A Kumar - vlsid, 2001 - computer.org
... approaches are [7], [3] and [5]. One of the important feature of their architectural model used in [3] and [7] is that it captures the differ- entiating features of the **instruction set** and special **...** For each architecture instance of the architecture **template**, a specific **simulator** is derived in **...**
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Simics: A full system simulation platform
PS Magnusson, M Christensson, J Eskilson, D ... - COMPUTER,, 2002 - computer.org
... Naturally, we wish to **simulate** an entire system and to do so with total accuracy—a perfect **...** Simics is also sufficiently **generic** to **model** embedded systems, desktop or **set**-top boxes, telecom **...** Simics simulates processors at the **instruction-set** level, including the full supervisor state **...**
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LISA---machine description language for cycle-accurate **models** of programmable DSP architectures psu.edu [PDF]
S Pees, A Hoffmann, V Zivojnovic, H ... - Proceedings of the 36th ..., 1999 - portal.acm.org
... HDLs) like VHDL or Ver- ilog are widely used to **model** and **simulate** processors, but **...** Texas Instruments, TMS32OC62x/C67x CPU and In- struction **Set** Reference Guide, Mar **...** D. Bradlee, R. Henry, and S. Eggers, "The Marion system for retargetable **instruction** scheduling," in Proc **...**
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[PDF] Generation of interpretive and compiled **instruction set** simulators psu.edu [PDF]
R Leupers, J Elste, B Landwehr - Proceedings of the ASP-DAC, 1999 - Citeseer
... or PC host, such tools have to be designed as cross-compilers or cross-simulators, respec- tively, which generate and **simulate** code for **...** The Insulin **instruction-set** simulator is part of the FlexWare system 5. It is based on a congurable VHDL **model** of a **"generic"** processor. **...**
Cited by 51 - Related articles - View as HTML - All 13 versions

A universal technique for fast and flexible **instruction-set** architecture simulation psu.edu [PDF]
A Nohl, G Braun, O Schliebusch, R Leupers, ... - Proceedings of the ..., 2002 - portal.acm.org
... and sequences the appropriate host operations that are required to **simulate** the application **...** A LISA **model** is a mixed structural/behavioral description of a proces- sor **...** The proces- sor's **instruction-set** including **instruction**-coding, assembly syntax, functional behavior, and timing **...**
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A novel methodology for the design of application-specific **instruction-set** processors (ASIPs) using a machine description language psu.edu [PDF]
A Hoffmann, T Kogel, A Nohl, G Braun, ... - ... on computer-aided ..., 2001 - ieeexplore.ieee.org
... HDLs like VHDL or Verilog are widely used to **model** and **simulate** processors, but **...** Considering **instruction-set** simulation, efficient runtime reduction can be achieved by per- forming repeatedly **...** tion-accurate **models**, it becomes a complex task for **models** with **instruction** pipelines **...**
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Hardware/software **instruction set** configurability for system-on-chip processors psu.edu [PDF]
A Wang, E Killian, D Maydan, C ... - Proceedings of the 38th ..., 2001 - portal.acm.org
... The simulator is able to correctly **simulate** an Xtensa program at close to one million instructions per second regardless of whether the simulated program uses TIE **...** "ISDL: An **instruction set** description language **...** "LISA - machine description language and **generic** machine **model ...**
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Asim: A performance **model** framework psu.edu [PDF]
J Emer, P Ahuja, E Borch, A Klauser, CK Luk, S ... - Computer, 2002 - ieeexplore.ieee.org
... The Aint feeder, the most aggressive in this **set** of **instruction** feeders,2 supplies **...** Aint fetches and executes any **instruction** under the direction of the performance **model**, but **...** Aint can help a performance **model** correctly **simulate** a modern, dynamically scheduled, speculative micro **...**
Cited by 156 - Related articles - BL Direct - All 17 versions

The M5 simulator: Modeling networked systems
N1 Binkert, RG Dreslinski, LR Hsu, KT Lim, AG ... - IEEE ..., 2006 - ieeexplore.ieee.org
... Using this language, a simple add **instruction** could be coded as Rc = Ra + Rb. A parser con- verts the ISA description to a **set** of instruc- tion classes, which include methods that **...** of warm-up time required for TCP to stabilize can be significantly larger than is practical to **simulate**. **...**
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A **generic** tool **set** for application specific processor architectures psu.edu [PDF]
F Engel, J Nührenberg, GP Fettweis - Proceedings of the eighth ..., 2000 - portal.acm.org
... During simulation a jump to the succeeding **instruction** sequence is necessary **...** As part of the M3-DSP chip **set** this processor is re- sponsible for pre- and post-processing **...** Hence to **simulate** cor- rect response times a cycle accurate **model** with full control of the pipeline behavior is **...**
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S Yoo, G Nicolescu, L Gauthier, A ... - Proceedings of the ..., 2002 - portal.acm.org
... SoCOS also enables to **model** final OSs with a **generic** OS simulation **model** [15]. **...** OS, the de- signer needs to run more accurate simulation such as using **instruction set** simulators **...** To **simulate** a specific OS implementation, the designer needs to do "personalization" of the virtual **...**
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